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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,406	07/27/2001	Saeeda Khankhel	IDF 1614 (4000-04800)	8871
28003	7590	02/07/2006	EXAMINER MERED, HABTE	
SPRINT 6391 SPRINT PARKWAY KSOPHT0101-Z2100 OVERLAND PARK, KS 66251-2100			ART UNIT 2662	PAPER NUMBER

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/916,406

Applicant(s)

KHANKHEL, SAEEDA

Examiner

Habte Mered

Art Unit

2662

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 November 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 and 5-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 5-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on 07-27-2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The amendment filed on 15 November 2005 has been entered and fully considered.
2. Claims 1-3 and 5-27 are currently pending.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claim 12** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation "a plurality of queues, each one of the queues having an input coupled in parallel with a corresponding one of the plurality of outputs of the non-re-circulating Batcher-sorter trap stage" is not clear as it contradicts with the support given in Figure 3B. In Figure 3-B, the inputs to queues 204 ... 213 are 211-1...211-L and are in series to the queues in question. It is not clear which output of the sorter and trap stage is in parallel with the input of the queues in question.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 1-3** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 4, 516, 238), hereinafter referred to as Huang, in view of Yang et al (US 5, 856, 977), hereinafter referred to as Yang.

Huang teaches a full access, non-blocking, wide band switching system in Figure 1 that is designed to switch signals that have destination addresses embedded in the signal structure. The system of Figure 1 comprises of a concentrator, a self-routing sorting network, a trap network, and a self-routing expander.

7. Regarding **claim 1**, Huang discloses a switching system for a telecommunications network (**See Figure 1**), comprising:

- a) a first stage having input and output sides, where the output side is concentrated relative to the input side (**See Column 5, Lines 7-11 and Lines 35-48; Figure 1, element 10**); and
- b) a second stage having input and output sides, where the input side of the second stage is coupled to the output side of the first stage and the output side of the second stage being comprised of a plurality of outputs (**See Column 5, Lines 10-14; Huang discloses that the first stage (i.e. concentrator) outputs collectively labeled as 1100 in Figure 1 is the input to the second stage and the second stage can be viewed as a stage that includes the sorter sub-network and the optional trap sub-network.**)

Huang, however, fails to teach aging each cell having a non-unique destination address in the second stage and that the second stage is a non-recirculating sort and trap stage.

Yang teaches a switch for transporting cells or packets without causing input, internal and output contention. Yang achieves a contention free switch by using a distribution network and shared buffers as a non-recirculating sort and trap stage.

Yang teaches a system wherein the second stage is a non-recirculating sort and trap stage. **(In Figure 10 element 110 is a sorter that can be a Batch-Banyan Network. See also Column 6, Line 25. Further in Figure 10, elements 120 are shared buffers and serve as a trap stage. This is further shown in Figure 11. See Column 6, Lines 46-50.)** Yang further discloses a plurality of cells arrive at the second stage, in a first time slot, the second stage placing each cell having a unique destination address on a selected one of the plurality of outputs and aging each cell having a non-unique destination address in a buffer connected in parallel with the outputs. **(See Column 7, Lines 10-26 and Figure 11. It is important to understand that the shared buffers collectively act as a trap stage. The shared buffers as illustrated in Column 7, Lines 20-22 and Column 8, Lines 49-50 age each cell having a non-unique destination address. Further as shown in Figure 10, the second stage i.e. the sort and trap stage is the combination of blocks 110 and 120 and the outputs of the second stage are the inputs of element 130. The Examiner would like to stress that Yang's apparatus teaches one ordinarily skilled in the art in order to handle output contention caused by cells having a non-unique destination address one only needs to age these cells in a shared output buffer. It is also obvious to one who is ordinarily skilled in the art a shared buffer has to be added**

to the second stage of Huang's switching system's so it can be shared by all of the outputs of the second stage.)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a shared buffer architecture to age cells causing output contention by having same destination address in the same time slot. The motivation to add the shared buffer architecture comes from the fact that Yang used such an arrangement to reduce switch hardware as shown in **Yang's Column 5, Lines 38-45**. An additional motivation is that Huang in Column 9, in Lines 9-11 and in Column 3, in Lines 49-50 indicates that cells having non-unique destination address are simply removed and does not adequately address on how to not drop cells having non-unique destination address. Both Yang and Huang were addressing on how to create a switching system that is free of output cell contention as shown in **Yang's Column 4, Lines 19-21 and Huang's Column 3, Line 40**.

8. Regarding **claim 2**, Huang discloses a switching system wherein the first stage is a concentrator. **(See Element 10 in Figure 1; Column 5, Lines 5-7)**

9. Regarding **claim 3**, Huang discloses a switching system wherein the first stage in Huang's switching system shown in Figure 1 is a concentrator and performs an N: L concentration on cells arriving in the first time slots. **(See Element 10 in Figure 1; Column 5, Lines 6-11 and Lines 34-52; Huang explains the need for a concentrator and shows why when having N input signals at the concentrator where only L of the non-adjacent N input signals are active at a time the output of**

the concentrator will be L adjacent active output signals where the non-active input signals are dropped and $L < N$)

10. **Claims 5-9, 22, 23, 26, and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Yang as applied to claim 1 above, and further in view of Cooperman et al (US 5, 862, 128), hereinafter referred to as Cooperman.

11. Regarding **claims 5, 8, and 22**, the combination of Huang and Yang discloses a switching system that has a second stage that comprises a sorter sub-stage for arranging the plurality of cells arriving at the second stage in a first time slot in a first order, where the first order is based upon the destination address. **(See Huang's Column 7, Lines 55-64 and Huang's Column 8, Lines 10-24; It is important to note that the combination of the sorter and trap networks can be viewed as constituting the second stage of Huang's switching system)**

The combination of Huang and Yang further discloses a trap substage for placing each cell having a unique destination address on the selected one of the plurality of outputs and aging each cell having a non-unique destination address. **(See Yang's Column 4, Lines 45-58)**

The combination of Huang and Yang further discloses in the next time slot the trap substage places the aged cells on the plurality of outputs if the non-unique destination address for the aged cells becomes unique in that next time slot. **(See Yang's Column 7, Lines 10-26)**

The combination of Huang and Yang, however, fails to disclose that the second stage needs to take into consideration the priority assigned to the incoming cells.

Cooperman teaches a system that improves existing switch architecture like that of Huang's by replacing the trap sub-network with a merged buffer architecture that is similar to Yang's architecture as shown in Figure 5.

Cooperman teaches that incoming cells are sorted and eventually routed to the appropriate output ports after taking into consideration the destination address and priority assigned to each of them. **(See Column 3, Lines 1-3 and 49-55; Column 4, Lines 27-32; and Column 5, Lines 8-24)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Huang's and Yang's switching system to incorporate a means and method to sort and route packets or cells based on priority. The motivation to sort and route on priority comes from the fact that a switching system can be an ATM switching system that supports different services with different quality of services (QoS) and priorities and to maintain the contracted QoS the switch has to process and route based on pre-assigned priorities. Yang's system is geared to ATM switching architecture as indicated in **Column 1, Lines 20-25**.

12. Regarding **claim 6**, both Huang and Yang teach the aforementioned invention, including the sorter sub-stage being a Batchier sorter. **(See Huang Column 7, Lines 65-68 and Yang Column 6, Lines 24-26)**

13. Regarding **claims 7, 26, and 27**, Huang disclosed the aforementioned invention but does not disclose a trap buffer in which cells having non-unique destination addresses for the first time are aged until the next time slot. Huang further does not disclose that the cells in the trap buffer consist essentially of cells with a non-unique

destination address. Huang also fails to indicate that each cell passes through the sorter and trap substage only once.

In Yang's switching system the aged cells with non-unique destination address are routed in the next time slot. **(See Column 7, Lines 22-26)**. Yang further discloses that the cells in the trap buffer consist essentially of cells with a non-unique destination address. **(See Column 4, Lines 51-54 and Column 7, Lines 20-22)**. Yang also discloses that all cells go through the distribution network that serves as the sorter and then go through the shared buffer that serves as the trap substage only once. **(See Figures 10 and 11 and Column 7, Lines 10-25)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a merged buffer architecture to age cells causing output contention by having same destination address in the same time slot in a specific buffer and to route them in the next time slot when the specific output becomes available. The motivation to add the merged buffer architecture comes from the fact that Yang used such an arrangement to reduce switch hardware as shown in **Yang's Column 5, Lines 38-45**. Both Yang and Huang were addressing on how to create a switching system that is free of output cell contention as shown in **Yang's Column 4, Lines 19-21 and Huang's Column 3, Line 40**.

14. Regarding **claims 9 and 23**, the combination of Huang and Yang teaches all aspects of the claimed invention as set forth in the rejection of claim 8 including:

a) a third stage having an input side comprised of a plurality of inputs, each input coupled to a corresponding one of the plurality of outputs of the second stage (**See Huang Column 5, Lines 18-29; Element 40 in Figure 1 and Figures 13-15.**)

b) wherein, in the first time slot and each one of a series of at least one subsequent time slots, the second stage placing a cell having a unique destination address on one of the plurality of outputs (**See Yang Column 7, Lines 10-26**)

The combination of Huang and Yang, however, fails to disclose that the system can be a multi-cast switching system.

Cooperman discloses that the switching system can be a multi-cast switching system (**See Cooperman Column 9, Line 11 and Figure 9**)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Huang's and Yang's switching system to incorporate multicast capability. The motivation is that Yang's system is an improvement over the existing St. Louis Switching fabric which already had multicasting capabilities as indicated in Yang's Column 3, Lines 50-55 and further multicasting is an essential feature for any improved switch to have.

15. **Claims 10-11 and 24-25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang in view of Yang and further in view of Cooperman and further in view of Widjaja et al (US 5, 440, 553), hereinafter referred to as Widjaja.

16. Regarding **claims 10 and 24**, the combination of Huang and Yang and Cooperman disclose all aspects of the claimed invention as set forth in the rejection of claim 9 including that the switch can be a multi-cast switching system (**See Cooperman**

Column 9, Line 11 and Figure 9). However the combination of Huang and Yang and Cooperman fails to teach that the third stage of the switch can comprise a queuing stage.

Widjaja teaches an output buffered packet multi-stage switch (**See Figures 3 and 4**) with priority packet transmission and flexible buffer management scheme. The switch in Figure 3 has a sorter and trap sub-stages and the output of the sorter and trap stage is fed to a queuing stage as shown in Figures 1a and 1b. (**See Column 3, Lines 63-68 and Column 4, Lines 1-9**).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the modified invention of Huang's and Yang's and Cooperman's switching system by incorporating a queuing stage, the motivation being achieving buffer efficiency while avoiding any potential lockout problem for systems that use shared buffering system as indicated in Widjaja's **Column 2, Lines 57-65**. Huang's and Yang's and Cooperman's system taken individually or in combination use shared buffer system.

17. Regarding **claims 11 and 25**, the combination of Huang and Yang and Cooperman disclose all aspects of the claimed invention as set forth in the rejection of claim 9 including that the switch can be a multi-cast switching system (**See Cooperman Column 9, Line 11 and Figure 9**) but fail to disclose that the queuing stage has a plurality of queues that matches the number of outputs of the switching system.

Widjaja teaches an output buffered packet multi-stage switch wherein the queuing stage further comprises a plurality of queues, each having an input coupled to

a corresponding one of the plurality of outputs of the second stage and system output; each one of the plurality of queues buffering cells having a common destination address to be output by the switching system. **(See Column 3, Lines 63-68 and Column 4, Lines 1-9; Figures 1a and 1b).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the modified invention of Huang's and Yang's and Cooperman's switching system by incorporating a queuing stage that has a plurality of queues that matches the number of outputs of the switching system, the motivation being achieving buffer efficiency while avoiding any potential lockout problem for systems that use shared buffering system as indicated in Widjaja's **Column 2, Lines 57-65**. Huang's and Yang's and Cooperman's system taken individually or in combination use shared buffer system.

18. **Claims 12-16**, as best understood in view of the above 112 2nd paragraph rejection, are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 4, 516, 238), hereinafter referred to as Huang, in view of Yang et al (US 5, 856, 977), hereinafter referred to as Yang, and Widjaja et al (US 5, 440, 553), hereinafter referred to as Widjaja.

19. Regarding **claim 12**, Huang discloses a high performance switching system, comprising of a concentrator stage having a plurality of input ports for the switching system and a plurality of outputs, where the concentrator concentrates cells entering the switch on the plurality of input ports and then routes the concentrated cells onto the plurality of outputs by discarding idle ones of the plurality of inputs **(See Huang Column**

5, Lines 5-11 and Lines 35-48; See Element 10 in Figure 1). Huang further discloses that a Batchersorter and trap stage having a plurality of inputs and a plurality of outputs, each of the plurality of inputs of the non-re-circulating Batchersorter trap stage coupled to a corresponding one of the plurality of outputs of the concentrator stage (**See Huang Column 5, Lines 10-14; Huang discloses that the first stage (i.e. concentrator) outputs collectively labeled as 1100 in Figure 1 is the input to the second stage. The second stage can be viewed as a stage that includes the sorter sub-network and the optional trap sub-network.)**

Huang fails to disclose that the switching system can have a non-re-circulating Batchersorter and trap stage. Huang fails to disclose that his switching system can have a queuing system as well as serve ATM platform.

Yang teaches that an ATM switching system (**Yang Column 1, Line 20-25**) can have a non-re-circulating Batchersorter and trap stage (**Column 7, Lines 10-26**). (**The shared buffers as illustrated in Column 7, Lines 20-22 and Column 8, Lines 49-50 age each cell having a non-unique destination address. Further as shown in Figure 10, the second stage i.e. the sort and trap stage is the combination of blocks 110 and 120 and the outputs of the second stage are the inputs of element 130. The Examiner would like to stress that Yang's apparatus teaches one ordinarily skilled in the art in order to handle output contention caused by cells having a non-unique destination address one only needs to age these cells in a shared output buffer. It is also obvious to one who is ordinarily skilled in the art a**

shared buffer has to be added to the second stage of Huang's switching system's so it can be shared by all of the outputs of the second stage.)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a non-re-circulating Batchersorter and trap stage in the form of a distribution network and merged buffer architecture to age cells causing output contention. The motivation to add a non-re-circulating Batchersorter and trap stage comes from the fact that Yang used such an arrangement to reduce switch hardware as shown in **Yang's Column 5, Lines 38-45**. An additional motivation is that Huang in Column 9, in Lines 9-11 and in Column 3, in Lines 49-50 indicates that cells having non-unique destination address are simply removed and does not adequately address on how to not drop cells having non-unique destination address. Both Yang and Huang were addressing on how to create a switching system that is free of output cell contention as shown in **Yang's Column 4, Lines 19-21 and Huang's Column 3, Line 40**.

Huang also fails to disclose that the modified switching system invention can have a third stage where the third stage is a queuing stage.

Widjaja teaches an output buffered packet multi-stage switch (**See Figures 3 and 4**) with priority packet transmission and flexible buffer management scheme. Widjaja discloses that the switching system has a plurality of queues and each one of the queues have an input coupled to a corresponding one of the plurality of outputs of the non-re-circulating Batchersorter trap stage and an output port for the switching system, and each one of the plurality of queues buffers cells exiting the switching

system which share a common destination address (**See Widjaja Column 3, Lines 63-68 and Widjaja Column 4, Lines 1-9; Figures 1a and 1b**).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Huang's switching system by incorporating a queuing stage, the motivation being achieving buffer efficiency while avoiding any potential lockout problem for systems such as Huang's that use shared buffering system as indicated in Widjaja's **Column 2, Lines 57-65**.

20. Regarding **claim 13**, Huang teaches a switching system that further comprises:

- a) a sorter sub-stage for ordering the plurality of cells arriving at the second stage in each one of the plurality of time slots based upon the destination address (**See Column 7, Lines 55-65**) and
- b) a trap substage for placing, during each one of the plurality of time slots, each one of the plurality of cells having either a unique destination address on a selected one of the plurality of outputs (**See Column 9, Lines 25-35**)
- c) for each one of the plurality of time slots, the trap substage selecting cells for placement on the plurality of outputs from a set of cells comprised of cells arriving from the sorter substage. (**See Column 5, Lines 14-20**)

Huang, however, fails to teach aging each cell having a non-unique destination address in the second stage and that the second stage is a non-recirculating sort and trap stage and that the cells causing output contention are sent in a different time slot.

Yang teaches a system wherein the second stage is a non-recirculating sort and trap stage. (**In Figure 10 element 110 is a sorter that can be a Batch-Banyan**

Network. See also Column 6, Line 25. Further in Figure 10, elements 120 are shared buffers and serve as a trap stage. This is further shown in Figure 11. See Column 6, Lines 46-50.) Yang further discloses a plurality of cells arrive at the second stage, in a first time slot, the second stage placing each cell having a unique destination address on a selected one of the plurality of outputs and aging each cell having a non-unique destination address. **(See Column 7, Lines 10-26 and Figure 11).** Yang also teaches that cells causing output contention are delayed and transmitted in a different time slot. **(See Column 7, Lines 22-26)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a non-re-circulating Batcher-sorter and trap stage in the form of a distribution network and merged buffer architecture to age cells causing output contention. The motivation to add a non-re-circulating Batcher-sorter and trap stage comes from the fact that Yang used such an arrangement to reduce switch hardware as shown in **Yang's Column 5, Lines 38-45**. Both Yang and Huang were addressing on how to create a switching system that is free of output cell contention as shown in **Yang's Column 4, Lines 19-21 and Huang's Column 3, Line 40**.

Huang, however, fails to disclose that the second stage needs to take into consideration the priority assigned to the incoming cells.

Widjaja teaches that incoming cells are sorted and eventually routed to the appropriate output ports after taking into consideration the destination address and priority assigned to each of them. **(See Column 6, Lines 30-35)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a means and method to sort and route packets or cells based on priority. The motivation to sort and route on priority comes from the fact that a switching system can be an ATM switching system that supports different services with different quality of services (QoS) and priorities and to maintain the contracted QoS the switch has to process and route based on pre-assigned priorities. Widjaja's system is geared to ATM switching architecture as indicated in **Column 2, Lines 5-10**.

21. Regarding **claim 14**, Huang discloses a switching system of wherein the concentrator stage performs N: L concentrations on arriving cells. **(See Element 10 in Figure 1; Column 5, Lines 6-11 and Lines 34-52; Huang explains the need for a concentrator and shows why when having N input signals at the concentrator where only L of the non-adjacent N input signals are active at a time the output of the concentrator will be L adjacent active output signals where the non-active input signals are dropped and $L < N$)**

22. Regarding **claim 15**, Huang discloses a switching system of wherein the sorter sub-stage is a Batchier sorter. **(Column 7, Lines 65-68)**

23. Regarding **claim 16**, Huang fails to disclose a switching system of wherein the trap sub-stage further comprises a trap buffer for aging cells with non-unique address.

Yang discloses a switching system of wherein the trap sub-stage further comprises a trap buffer for aging cells with non-unique address. **(See Column 7, Lines 10-25)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Huang's switching system to incorporate a merged buffer architecture to age cells causing output contention by having same destination address in the same time slot. The motivation to add the merged buffer architecture comes from the fact that Yang used such an arrangement to reduce switch hardware as shown in **Yang's Column 5, Lines 38-45**. Both Yang and Huang were addressing on how to create a switching system that is free of output cell contention as shown in **Yang's Column 4, Lines 19-21 and Huang's Column 3, Line 40**.

22. Claims **17 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al (US 4, 542, 497), hereinafter referred to as A. Huang, in view of Yang et al (US 5, 856, 977), hereinafter referred to as Yang.

*A. Huang discloses a multi-cast switching system in **Figure 6** that has a broadcast network stage consisting of source sorting sub-stage and copy sub-stage. The source sorting sub-stage, which is element 4 in Figure 6, sorts incoming cells on the source address and feeds it to the copy sub-stage, which is element 42 in Figure 6. Thus, at the outputs of the sorting network, the original cells and the associated empty copy cells with the same source address appear contiguously. The copy sub-stage then replicates the data in each source cell and inserts this data into the data fields of the associated empty copy cells. (See A. Huang Column 3, Lines 25-50)*

25. Regarding **claim 17**, the multi-cast switching system disclosed by A. Huang, comprises a broadcast network having input and output sides, the broadcast network receives, on its input side, a plurality of source cells from at least one source and a

plurality of empty copy cells, the broadcast network copies data from selected ones of the plurality of source cells and inserts this data in the empty copy cells to produce copies of the source cells **(See A. Huang Column 9, Lines 35-55 and Column 11, Lines 5-10)**

A. Huang discloses that the inputs to the broadcast network consisting of the source sorting and copying sub-stages are source and empty copy cells. **(See A. Huang Column 3, Lines 25-50 and Column 9, Lines 35-55)**

A. Huang fails to teach a switching system with a non-circulating Batcher sort-trap stage.

Yang teaches a switching system that has a non-re-circulating Batcher sort-trap stage having input and output sides. **(See Column 7, Lines 10-25 and Figures 10 and 11)** Yang further discloses a plurality of cells arrive at the second stage, in a first time slot, the second stage placing each cell having a unique destination address on a selected one of the plurality of outputs and aging each cell having a non-unique destination address in a buffer connected in parallel with the outputs. **(See Column 7, Lines 10-26 and Figure 11. It is important to understand that the shared buffers collectively act as a trap stage. The shared buffers as illustrated in Column 7, Lines 20-22 and Column 8, Lines 49-50 age each cell having a non-unique destination address. Further as shown in Figure 10, the second stage i.e. the sort and trap stage is the combination of blocks 110 and 120 and the outputs of the second stage are the inputs of element 130. The Examiner would like to stress that Yang's apparatus teaches one ordinarily skilled in the art in order to handle**

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output contention caused by cells having a non-unique destination address one only needs to age these cells in a shared output buffer. It is also obvious to one who is ordinarily skilled in the art a shared buffer has to be added to the second stage of Huang's switching system's so it can be shared by all of the outputs of the second stage.)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify A. Huang's switching system to incorporate a non-circulating shared buffer architecture to age cells causing output contention by having the same destination address in the same time slot. The motivation is that Huang in Column 9, in Lines 9-11 and in Column 3, in Lines 49-50 indicates that cells having non-unique destination address are simply removed and does not adequately address on how to not drop cells having non-unique destination address. The additional motivation to add the shared buffer architecture comes from the fact that Yang used such an arrangement to reduce switch hardware as shown in **Yang's Column 5, Lines 38-45**.
26. Regarding **claim 18**, A. Huang discloses a multi-cast switching system wherein the broadcast network further comprises:

- a) a source sort stage for sorting source and copy packets entering the source sort stage based upon a data source identifier for each one of the plurality of source packets and the plurality of copy packets (**See Column 10, Lines 57-65**); and
- b) a copy stage for copying data from source packets containing a first data source identifier to copy packets containing the first data source identifier. (**See Column 11, lines 5-10**)

27. **Claims 19-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over A. Huang in view of Yang as applied to claim 17 above, and further in view of Cooperman et al (US 5, 862, 128), hereinafter referred to as Cooperman.

28. Regarding **claim 19**, A. Huang discloses a multi-cast switching system but fails to disclose a non-recirculating Batcher sort-trap stage.

Yang discloses a non-recirculating Batcher sort-trap stage that further comprises:

- a) a sorter for arranging a plurality of cells arriving at the second stage in the first time slot in a first order where the first order is based on destination address for each arriving cell; **(Figure 10, element 110; Column 7, Lines 1-10)**
- b) a trap sub-stage for placing each cell with unique destination address on a selected output of the plurality of outputs and aging each cell having a non-unique destination address; **(Column 7, Lines 10-25)**
- c) wherein, in a next time slot, the trap sub-stage will place the aged cells on selected outputs of the plurality of outputs if the non-unique destination address for the aged cells become unique in that time slot. **(Column 7, Lines 22-26)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify A. Huang's switching system to incorporate a non-recirculating Batcher-sorter and trap stage in the form of a distribution network and merged buffer architecture to age cells causing output contention. The motivation to add a non-re-circulating Batcher-sorter and trap stage comes from the fact that Yang used such an arrangement to reduce switch hardware as shown in **Yang's Column 5, Lines 38-45**.

A. Huang, however, also fails to disclose that the second stage needs to take into consideration the priority assigned to the incoming cells.

Cooperman teaches that incoming cells are sorted and eventually routed to the appropriate output ports after taking into consideration the destination address and priority assigned to each of them. **(See Column 3, Lines 1-3 and 49-55; Column 4, Lines 27-32; and Column 5, Lines 8-24)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify A. Huang's switching system to incorporate a means and method to sort and route packets or cells based on priority. The motivation to sort and route on priority comes from the fact that a switching system can be an ATM switching system that supports different services with different quality of services (QoS) and priorities and to maintain the contracted QoS the switch has to process and route based on pre-assigned priorities. Yang's system is geared to ATM switching architecture as indicated in **Column 1, Lines 20-25**.

29. Regarding **claim 20**, A. Huang discloses a multi-cast switching system wherein the sub-stage is a Batchier sorter. **(See A. Huang Column 10, Line 67)**

30. Regarding **claim 21**, A. Huang teaches all aspects of the claimed invention as set forth in the rejection of claim 19 but fails to disclose a multi-cast switching system wherein the trap substage further comprises a trap buffer in which those cells having non-unique destination addresses for the first time are aged until the next time slot.

Yang discloses a trap stage consisting of a trap buffer in which those cells having non-unique destination addresses for the first time are aged until the next time slot.

(See Column 7, Lines 10-25)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify A. Huang's switching system to incorporate a merged buffer architecture to age cells causing output contention by having same destination address in the same time slot. The motivation to add the merged buffer architecture comes from the fact that Yang used such an arrangement to reduce switch hardware as shown in **Yang's Column 5, Lines 38-45.**

Response to Arguments

31. Applicant's arguments filed on 15 November 2005 have been fully considered but they are not persuasive.

32. Applicant, in the Remarks on pages 11 and 12, argues that the Examiner has not provided adequate motivation with respect to amended independent claims 1, 12, and 17 when combining Huang I and Huang II with Yang. Examiner respectfully disagrees with Applicant's conclusions. The rejections for these claims adequately discuss the motivations. In summary Huang I and Huang II indicate the need to have a trapping stage to address cells with non-unique address by simply removing them. There is no indication what is done with the removed packets – Are they recirculated? Are they simply dropped? Or are they aged? In Huang et al (US 4, 516, 238) there is even suggestion of aging a cell using a "trap" flag in Column 9, Line 30. Neither Huang I nor Huang II suggest or teach a recirculating trap stage. Yang adequately teaches that

aging cells having non-unique address in a shared buffer solves output contention caused by these cells, which is the basis of a non-recirculating trap stage.

33. Applicant, in the Remarks on page 14 in lines 7-11, argues that Yang's shared buffers are connected in series and not in parallel and fails to teach the limitations cited in claims 1, 12, and 17. Examiner respectfully disagrees with Applicant's conclusion. The Examiner would like to stress that Yang's apparatus teaches one ordinarily skilled in the art in order to handle output contention caused by cells having a non-unique destination address one only needs to age these cells in a shared output buffer. It is also obvious to one who is ordinarily skilled in the art a shared buffer has to be added to the second stage of Huang's switching system's so it can be shared by all of the outputs of the second stage. The easy way to connect a shared buffer to all outputs is in parallel.

34. Applicant, in the Remarks on page 14 in the last paragraph, with respect to claim 27 Applicant argues Yang's shared buffer contains cells with both unique and non-unique destinations addresses. Examiner respectfully disagrees with Applicant's conclusion. Yang specifically indicates that the routing algorithm will allocate all of the conflicting cells destined for the same output port are sent to the same shared buffer as illustrated in Column 7, Lines 20-21 and in Column 8, Lines 49-50. This is central concept behind a non-circulating trap stage and is adequately taught by Yang.

Conclusion

35. Applicant's amendment necessitated the new ground(s) of rejection (including the 112 2nd paragraph rejection of claim 12 based on new introduced limitation) presented

in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patent is cited to show the state of the art for copy network for multicast packet switching:

U. S. Patent (4, 813, 038) to Lee


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571 272 3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2662

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HM
02-06-2006



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